REMARKS

This application has been carefully reviewed in light of the office action mailed November 20, 2002. New claims 26-33 have been added. Claims 1-11 and 26-33 are pending in this application. Applicants respectfully request early and favorable acceptance of this application.

Objections under 37 C.F.R 1.83

The drawings are objected to under 37 C.F.R 1.83(a) as not showing every feature of the invention specified in the claims. The examiner states that the origin or nature of the "extra" layer lining the trench adjacent to the layer (e.g., 95 of Fig. 4) in Fig.'s 4 and 6 is not recited in the specification or the claims. Applicant respectfully traverses the objection.

Fig. 3 shows dielectric material (e.g., 60) filling the recessed region (e.g., 20), which is subsequently etched to form recessed region or trench (e.g., 76) as shown in Fig. 4 and recited in paragraphs 17 through 23 of the specification. Claim 1 recites among other things; a first dielectric material (e.g., 60) deposited in a first recessed region (e.g., 20) and formed with a second recessed region (e.g., 76) also recited in paragraphs 17 through 23 of the specification.

Fig. 4 also shows dielectric material (e.g. 95) deposited on the walls (e.g., 92) of the trench to provide reinforcement for additional stability under stress and to reduce defects as recited in paragraph 24. Claim 7 recites among other things; the recessed region formed having dielectric material (e.g., 95) deposited on the walls (e.g., 92) also recited in paragraph 24 of the specification. Thus both the specification and the claims are believed to

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be clear in the origin and nature of the "extra" layer in question, that is, dielectric material 60 and 95 of Fig.'s 4 and 6.

However, to improve the clarity of the origin and nature of dielectric material 60 of Fig.'s 4 and 6, applicant requests the examiner to approve the changes made in red (circled) per 37 CFR 1.121(d) to the attached drawing as follows:

a descriptor lead line 60 and descriptor 60 on the drawing in figure 4 (circled) have been added to further clarify the origin and nature of the layer shown.

a descriptor lead line 95 on the drawing in figure 4 (circled) have been added to further clarify the origin and nature of the layer shown. These changes do not introduce any new matter.

Thus applicant believes the objection to have been overcome.

Rejections under 35 USC §103

Claims 1-11 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent 5,640,041 issued to Lur et al. (hereinafter Lur '041) in view of U.S. Patent 5,308,786 issued to Lur et al. (hereinafter Lur '786).

Claim 1 recites among other things, a semiconductor device (e.g., 2) comprising a first dielectric material (e.g., 60) deposited in a first recessed region and formed with a second recessed region (e.g., 76), and a second dielectric material (e.g., 100) thermally grown over the first dielectric material to seal the second recessed region.

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The Lur '041 reference discloses in Fig. 6 trenches 19 formed in deposited silicon dioxide 24, and sealed with a layer 25 of chemical vapor deposition (CVD) silicon dioxide to form voids 30. The Lur '786 reference a similar device with narrow trenches 17 (Fig. 6) formed to a depth of two microns.

The examiner states on page 3 of the office action that a thermally grown and CVD silicon dioxide layer are functionally equivalent in terms of sealant atop trenches. Applicant respectfully traverses this argument as there are inherent property differences between thermally grown silicon dioxide and deposited silicon dioxide that result in producing voids having significant structural differences with corresponding device advantages.

For example, as the Lur '041 seal is formed by depositing a material (i.e., silicon dioxide) having poor step coverage (column 5 lines 9-21), material is also deposited in the trench (as shown in all Lur figures), which results in Lur's voids having decreased gaseous volume thus a higher dielectric constant. In contrast, the thermally grown dielectric material of the applicant does not grow in the trench, thus the voids of the applicant have increased gaseous volume which produces devices having correspondingly lower dielectric constant.

Furthermore, the Lur references are silent on the problem presented by depositing sealing material in the trench resulting in reduced volume, instead teaching filling the Lur trench "partially" or "completely" with deposited material (in column 5 lines 10-11 of the Lur '041 reference, and column 5 lines 20-24 of the Lur '786

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reference) which would decrease void volume, and therefore increase the effective dielectric constant.

Moreover, the Lur '041 reference teaches away from thermally grown dielectrics as a functional equivalent to deposited silicon dioxide in that the Lur sealant is purposefully chosen to have a "bad step coverage of between about 20 to 80%" (column 5, lines 5-20). Thermally grown dielectrics inherently provide near 100% step coverage as a result of their formation mechanism, as described in Microchip Fabrication, by Peter Van Zant, 3rd Edition, ISBN 0-07-067250-4, pages 143-150, a copy of which is attached to this amendment. Therefore, there would be no motivation to modify the Lur references by substituting a thermally grown silicon dioxide for deposited silicon dioxide, as the intended function, that is "bad step coverage", would be destroyed.

Therefore, claim 1 is not anticipated by the Lur references. Claims 2-11 depend from claim 1, and are therefore allowable for at least the same reasons.

New claim 26 recites among other things, a semiconductor device comprising a first dielectric material (e.g., 60) deposited in a first recessed region (e.g., 20) and formed with a second recessed region (e.g., 76), a first semiconductor layer (e.g., 75) deposited over and between the second recessed region, and a second dielectric material (e.g., 100) thermally grown on the first semiconductor layer to seal the second recessed region.

As discussed above, the Lur references disclose trenches formed in deposited silicon dioxide and sealed with deposited silicon dioxide to form voids.

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For reasons similar to those above, neither of the Lur references, whether alone or in combination, show or teach a semiconductor layer deposited over and between a recessed region and a dielectric layer thermally grown on the semiconductor layer to seal the recessed region as does the applicant.

Both of the Lur references seal the narrow trench by depositing dielectric directly onto dielectric material in which the trench are formed. In contrast, the sealing of the recessed region of the applicant is accomplished by thermally growing dielectric material on the semiconductor material layer as shown in Fig.'s 4-6 and taught in paragraph [0027] of the specification. As above, thermally growing silicon dioxide is believed to be patentably distinct from depositing silicon dioxide. Additionally, the semiconductor layer laterally expands when thermally converted to a dielectric layer, e.g., silicon dioxide, (refer to paragraph [0022] of the specification) thereby sealing the recessed region more quickly, as oxide grows more rapidly on polysilicon than on silicon (p. 149, Van Zant). There is no Lur semiconductor layer promoting lateral growth, thus the Lur trenches have dielectric material deposited within them, reducing the volume and decreasing the effective dielectric constant.

For the foregoing reasons, new claim 26 is believed to be patentably distinct from the references cited, and therefore new claim 26 should be in condition for allowance. Since new claims 27-33 depend from new claim 26, they should be allowable for at least the same reasons.

Applicants respectfully believe the rejection to have been overcome.

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Attached hereto is a marked up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "Version with markings to show changes made."

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Conclusion

Applicants respectfully request entry of this amendment and early and favorable acceptance of this application.

No fees are believed due by filing this Amendment. However, the Commissioner is hereby authorized to charge any fees due or credit any overpayment to Deposit Account - 501086.

If there are matters that can be discussed by telephone to further the prosecution of this application, applicants invite the examiner to call the undersigned attorney at the examiner's convenience.

Respectfully submitted,

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Version with Marking to Show Changes Made

IN THE CLAIMS

Please add new claims 26-33 as follows.

26. (New) A semiconductor device, comprising:

a semiconductor substrate having a surface formed with a first recessed region;

a first dielectric material deposited in the first recessed region and formed with a second recessed region;

a first semiconductor layer deposited over the first dielectric material; and

a second dielectric material thermally grown on the first semiconductor layer to seal the second recessed region.

27. (New) The semiconductor device of claim 26, wherein the first semiconductor layer includes deposited polysilicon.

28. (New) The semiconductor device of claim 27, wherein the second dielectric material includes thermally grown silicon dioxide.

29. (New) The semiconductor device of claim 26, further comprising an active device formed in an active region of the semiconductor substrate.

30. (New) The semiconductor device of claim 26, further comprising an electrical component formed over the second recessed region.

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31. (New) The semiconductor device of claim 30, wherein the electrical component comprises a passive device or bonding pad of the semiconductor device.

32. (New) The semiconductor device of claim 26, wherein the second recessed region is formed having a third dielectric material deposited on the walls.

33. (New) The semiconductor device of claim 32, wherein the third dielectric material includes silicon nitride.

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